Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.110”**

**.110”**

**Top Material: Al**

**Backside Material: NiAg**

**E = .021 X .024”**

**B = .024 X .042”**

**Backside Potential: COLLECTOR**

**Mask Ref: CP527**

**APPROVED BY: DK DIE SIZE .110” X .110” DATE: 9/8/21**

**MFG: CENTRAL THICKNESS .011” P/N: 2N6042**

**DG 10.1.2**

#### Rev B, 7/1